

REMARKS/ARGUMENTS

Claims 1-9 are pending in the Application. By this Amendment, claims 1 and 5 are being amended to improve their form. No new matter is involved.

In Paragraph 4 which begins on page 2 of the Office Action, claims 1-4 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,239,366 of Hashimoto. In Paragraph 5 on page 3 of the Office Action, claims 1-4 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,157,080 of Tamaki et al. In Paragraph 6 which begins at the bottom of page 3 of the Office Action, claims 1 and 2 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 6,321,734 of Kaminaga et al. In Paragraph 7 which begins on page 4 of the Office Action, claims 1-6 and 8 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 6,133,637 of Hikita et al. In Paragraph 9 which begins at the bottom of page 5 of the Office Action, claims 7 and 9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,133,637 of Hikita et al. in view of U.S. Patent 5,930,599 of Fujimoto et al. These rejections are respectfully traversed, particularly in view of the amendments being made to independent claims 1 and 5 herein.

The present invention is characterized in that no connection terminals such as solder balls are provided between one surface of the semiconductor chip (semiconductor substrate) and the support substrate, and further in that the semiconductor chip and the support substrate are bonded with resin containing microparticles, the maximum particle diameter of which is smaller than a distance between the semiconductor chip and the support substrate.

In contrast, none of the cited references, including Hashimoto, Tamaki, Kaminaga, Hikita or Fujimoto, disclose or suggest a structure wherein connection terminals such as solder balls are provided between one surface of a semiconductor

chip and a support substrate. In such a structure, the connection terminals such as solder balls are sufficiently larger than the microparticles (fillers) contained in the resin. As such, the cited references do not anticipate any need in relation to the distance separating the semiconductor chip from the support substrate to the particle diameter of the microparticles contained in the resin. More specifically, the cited references do include any disclosures or suggestions that would make possible conception of the characteristic feature according to the present invention. Accordingly, the present invention as claimed herein is submitted to clearly distinguish patentably over such references.

Claim 1 defines a semiconductor integrated device which is provided with a semiconductor chip on which a semiconductor integrated circuit is formed and a support substrate laminated on at least one surface of the semiconductor chip. As amended herein, the semiconductor integrated device is characterized in that "no connection terminals are provided between the surface of the semiconductor chip and the support substrate". In the semiconductor integrated device, resin that is a mixture of microparticles is filled between the semiconductor chip and the support substrate, and a distance between the semiconductor chip and the support substrate is larger than the maximum particle diameter of the microparticles.

Claims 2-4 depend from and contain all of the limitations of claim 1, so that such claims are also submitted to clearly distinguish patentably over the cited references.

In the case of claim 5, such claim defines a method of manufacturing a semiconductor integrated device which includes first and second steps. The first step is that of coating resin mixed with microparticles on at least one surface of a semiconductor substrate on which a semiconductor integrated circuit is formed, and laminating a support substrate on the semiconductor substrate to hold the resin

between the two substrates. In the second step, the support substrate is pushed against the semiconductor substrate. The method of claim 1 is further characterized in that "no connection terminals are provided between the surface of the semiconductor substrate and the support substrate". In the second step, the support substrate is pushed against the semiconductor substrate while keeping a distance between the semiconductor substrate and the support substrate larger than the maximum particle diameter of the microparticles. Accordingly, claim 5 is submitted to clearly distinguish patentably over the cited references.

Claims 6 and 7 depend from and contain all of the limitations of claim 5, so that such claims are also submitted to clearly distinguish patentably over the cited references.

Claim 8 defines a method of manufacturing a semiconductor integrated device which includes a first step of coating a first resin layer mixed with microparticles on at least one surface of a semiconductor substrate on which a semiconductor integrated circuit is formed. In a second step according to the method of claim 8, the first resin layer is hardened. In a third step, a second resin layer not containing microparticles is coated on the first resin layer which is hardened in the second step. In the second step, hardening is carried out so that the film thickness of the first resin layer after hardening is kept larger than the maximum particle diameter of the microparticles. Consequently, claim 8 is submitted to clearly distinguish patentably over the cited references.

Claim 9 depends from and contains all of the limitations of claim 8, so that such claim is also submitted to clearly distinguish patentably over the prior art.

In conclusion, claims 1-9 are submitted to clearly distinguish patentably over the cited references for the reasons discussed herein. Therefore, reconsideration and allowance are respectfully requested.

Appl. No. 10/773,088
Amdt. Dated October 20, 2005
Reply to Office Action of August 24, 2005

Attorney Docket No. 81784.0301
Customer No.: 26021

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
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Date: October 20, 2005

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